OP5142 PCIe Reconfigurable platform with RT-XSG toolbox support

User Guide

RTXSG-UG-11-04

I M A G I N A T I O N

T O

R E A L - T I M E

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1 Introduction

1.1 About the OP5142 PCIe Reconfigurable Platform from Opal-RT Technologies

The OP5142 (Figure 1) is one of the key building blocks in the modular OP5000 I/O system from Opal-RT Technologies. It allows the incorporation of FPGA technologies in RT-LAB simulation clusters for distributed execution of HDL functions and high-speed, high-density digital I/O in real-time models. Based on the highest density Xilinx Spartan-3 FPGAs, the OP5142 can be attached to the backplane of an I/O module of either a Wanda 3U- or Wanda 4U-based Opal-RT simulation system. It communicates with the target PC via a PCI-Express ultra-low-latency real-time bus interface.

The OP5142 includes connectivity to up to four (4) 4U digital and/or analog I/O conditioning modules. This allow the incorporation of task-specific I/O hardware, such as high-speed analog signal capture and generation.

Furthermore, FPGA developers can incorporate their own functionality, using the System Generator for DSP toolbox or their favorite HDL development tool, through the PCIe interface without the need for connecting to the JTAG interface. Configuration files can be uploaded and stored on the built-in Flash memory for instant startup.

The PCI-Express port on the OP5142 adapter board allows the user to connect the distributed processors together and operate at faster cycle times than ever before. This real-time link takes advantage of the FPGA power to deliver up to 2.5 Gbits/s full-duplex transfer rates.

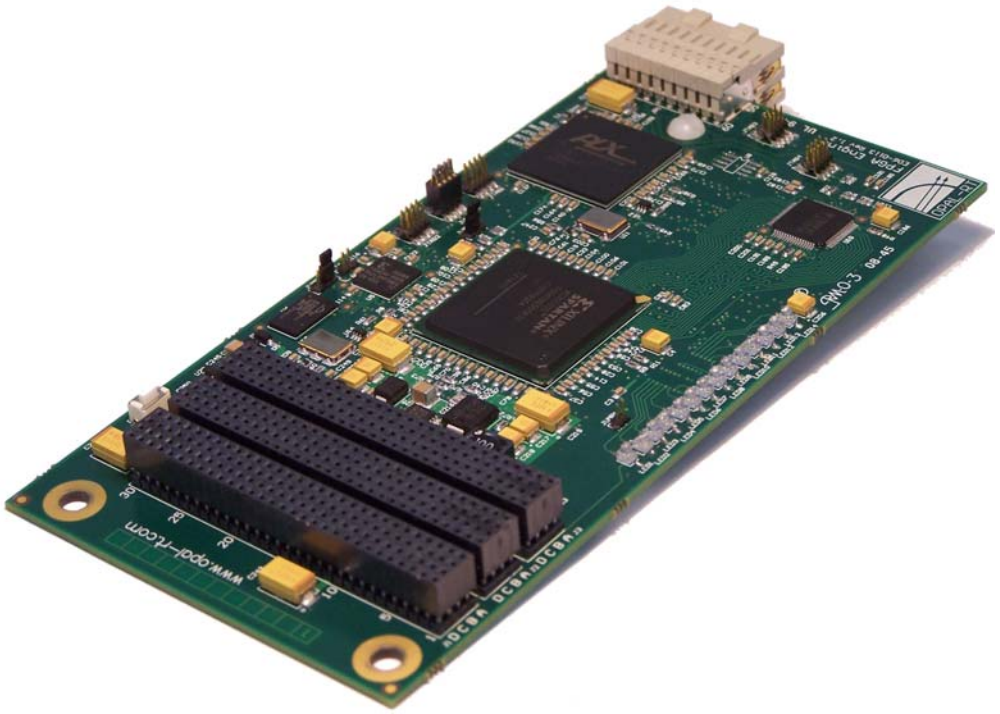

Figure 1:The OP5142 Reconfigurable board.

1.2 Key Features

Reconfigurability

The OP5142 platform FPGA device can be configured exactly as required by the user. Integration with Simulink, the System Generator for DSP toolbox from Xilinx and RT-XSG from Opal-RT Technologies allows the transfer of Simulink submodels to the OP5142 FPGA processor for distributed processing.

In addition, standard and user-developed functions can be stored on the on-board Flash memory for instant start-up. The OP5142 board is configurable on-the-fly using the PCIe bus interface and the RT-Lab/Livelab design environments.

Performance

OP5142 series products enable update rates of 100 MHz, providing the capability to perform time-stamped capture and generation of digital events for high precision switching of items such as PWM I/O signaling up to very high frequencies, as I/O scheduling is performed directly on the OP5142 board.

Channel Density

- Up to 256 software-configurable Digital I/O lines for event capture/generation, PWM I/O and user functions;
- Up to 128 16-bit Analog I/O channels, simultaneous sampling at 1 MS/s per channel for digital-to-analog conversion and 400 kS/s for analog-to-digital conversion.

1.3 Intended Audience and Required Skills and Knowledge

The intended user of the OP5142 platform in conjunction with the RT-XSG toolbox is a R&D, Algorithm or Test Engineer that needs a reconfigurable, very-high-speed, portable and low-cost processing unit with good analog and/or digital I/O capabilities.

1.3.1 Hardware description language (HDL) and fixed-point numbering

With the help of Xilinx System Generator for DSP toolbox, only minimal programmable logic technical knowledge is needed to use the OP5142 board. This blockset is used to translate a Simulink design built using particular library blocks into HDL. The translated design is used by Opal-RT tools to give access to I/O interfaces and debugging facilities.

However, the user should be familiar with the fixed-point numerical format and fixed-point data processing. The use of floating point numbers is very heavily resource consuming into FPGA processing devices and is in general not suitable in RT-XSG devices as the interface to the conversion modules is in a fixed-point format. A minimal training on FPGA architecture is also recommended.

1.3.2 Simulink

Simulink is a software package developed by the Mathworks that enables modeling, simulation and analysis of dynamic systems. Models are described graphically, following a precise format based on a library of blocks. RT-XSG uses Simulink to define models that will be executed by the reconfigurable platform. It is expected that the user has a clear understanding of Simulink operation, particularly regarding the model definition and simulation parameters.

1.4 Organization of this Guide

This document is the user guide. The topics covered are:

- **Introduction on page 1**- Provides an introduction to simulation and the principles behind the use of the OP5142 platform with Opal-RT I/O interfaces.
- **Requirements on page 5** - Software/hardware requirements for the use of the OP5142 platform with Opal-RT I/O interfaces.
- **Installation on page 7** - Procedure to install the OP5142 platform with Opal-RT I/O interfaces libraries and hardware.
- **Hardware description and setup on page 9** - Describes the hardware components related to the OP5142 platform.
- **Building models with the RT-XSG toolbox on page 13** - Describes the procedure to generate a configuration file for the OP5142 Platform using the Simulink-based editor and simulator, RT-XSG.

1.5 Conventions

Opal-RT guides use the following conventions:

Table 1: General and Typographical Conventions

THIS CONVENTION	INDICATES
Bold	User interface elements, text that must be typed exactly as shown.
Note:	Emphasizes or supplements parts of the text. You can disregard the information in a note and still complete a task.
Warning:	Describes an action that must be avoided or followed to obtain desired results.
Recommendation:	Describes an action that you may or may not follow and still complete a task.
Code	Sampel code.
Italics	Reference work titles.
Blue Text	Cross-references (internal or external) or hypertext links.

Requirements

2

2.1 Software requirements

The OP5142 PCIe Reconfigurable Platform needs the following softwares in order to be able to generate a programming file for the reconfigurable device and to program the platform:

Minimal configuration (with RT-XSG support):

- Microsoft Windows XP (32-bit version);
- Xilinx ISE design suite v10.1[1];
- Xilinx System Generator for DSP v10.1 or later (See footnote 1.);
- Matlab R2007b or R2008a.

Recommended configuration (with RT-XSG support):

- Microsoft Windows XP (32-bit version);
- Xilinx ISE design suite v10.1.03 with IP Update 3 or later (See footnote 1.);
- Xilinx System Generator for DSP v10.1.03 or later (See footnote 1.);
- Matlab R2007b or R2008a.

2.2 Hardware requirements

Minimal configuration

- A RT-LAB-compatible Wanda 3U or Wanda 4U target computer with a free PCIe bus slot;
- One Wanda Backplane Adapter as an interface between the OP5142 board and the target PC I/O module;
- One PCI-Express interface board and cable as an interface between the OP5142 board and the target PC PCIe bus;
- Refer to the third-party software documentation for host computer minimal hardware configuration.

1.Xilinx ISE Design Suite, IP and System Generator for DSP should always correspond to the latest available update. In particular, compatibility issues require that the installed release of each component to match (e.g. ISE Design Suite 10.1.03 with IP Update 3 and System Generator 10.1.03, or any later matching release of all the subcomponents). Updating one of the Xilinx subcomponents is likely to require an update of all other Xilinx tools and libraries to ensure full software compatibility.

Installation

3

Three steps must be performed to install the product, assuming that all the required third-party softwares are already installed:

1. Install the RT-XSG toolbox by running the installer. Follow the on-sceen instructions. After the installation, the following folders are created:

   - <RTXSG_ROOT>/Docs: Documentation folder;
   - <RTXSG_ROOT>/Common/libfpga: Hardware description folder (contains files necessary for the synthesis of the base configuration of the board);
   - <RTXSG_ROOT>/Simulink: Opal-RT RT-XSG Toolbox folder;
   - <RTXSG_ROOT>/Examples: Contains example user models.

   The installation also added the toolbox folders to the Matlab path and added the following files in the Matlab toolbox directory:

   - <Matlab installation directory>/toolbox/local/startup.m
   - <Matlab installation directory>/toolbox/local/setup_rtxsg.m

   Finally, an environment variable is created in your operating system:

   - RTXSG_ROOT=<RTXSG_ROOT>, where <RTXSG_ROOT> is your installation directory.

2. Connect the OP5142 board to the target computer as as described below:

   - Power-off the target computer;
   - Locate the target PC I/O module and connect the following boards, one over the other, using the appropriate connectors: (1) the Wanda Backplane Adapter; (2) the OP5142 PCIe Reconfigurable Platform; (3) the PCI-Express interface board;
   - Connect the PCIe cable from the PCI-Express interface board to one of the the target PC PCIe slot
   - If applicable, connect the RTSI cable from the PCI-Express interface board to the master synchronizing source (id the OP5142 is a slave) or its dependent slaves (if the OP5142 is the synchronization master);
   - Connect the target computer to the network;
   - Power-on the target computer.

Hardware description and setup

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4.1 OP5142 PCIe reconfigurable Platform

This active, FPGA-based board allows high-density digital I/O signaling, high-precision event capture and high-speed analog interfaces. It features a PCIe bus interface.

- Programmable Xilinx Spartan-3 xc3s5000 FPGA processor board for internal installation;
- Up to 256 software-configurable digital I/O lines for event capture/generation, PWM I/O and user functions;
- Up to 128 16-bit Analog I/O channels, simultaneous sampling at 1 MS/s for digital-to-analog conversion and 400 kS/s for analog-to-digital conversion, (located on optional I/O modules);
- PCIe port for ultra-low-latency data communications;
- Library of drag-and-drop RT-LAB blocks for Simulink.

The OP5142 allows the incorporation of FPGA technologies in RT-LAB simulation clusters for distributed execution of HDL functions and high-speed, high-density digital I/O in real-time models. Based on the highest density in the Xilinx Spartan-3 FPGA, the OP5142 can be attached to the I/O module backplane in either a Wanda 4U or Wanda 3U chassis, communicating with the target PC via the PCIe ultra-low-latency real-time bus interface.

4.2 Connectivity

Opal-RT provides an easy way to acquire and generate analog and digital signals. Analog and digital I/O signals are accessed via the Wanda Backplane interface board. Four 4U backplane slots are available, each of them giving access to a 96-pin front panel connector to which can be attached either:

- Two banks of up to 32 digital lines, each bank being either in the inbound or ouound direction.
- Two banks of 16 differential analog signals. Each bank can be configured to give access to input or output analog signals. These banks are interfaced with interchangeable 16-channel analog conversion mezzanine modules placed on a passive carrier.

Refer to the library block description for details on compatible devices and on how to implement custom designs interfacing them. A block diagram of the OP5142 connectivity features is presented in Figure 2.

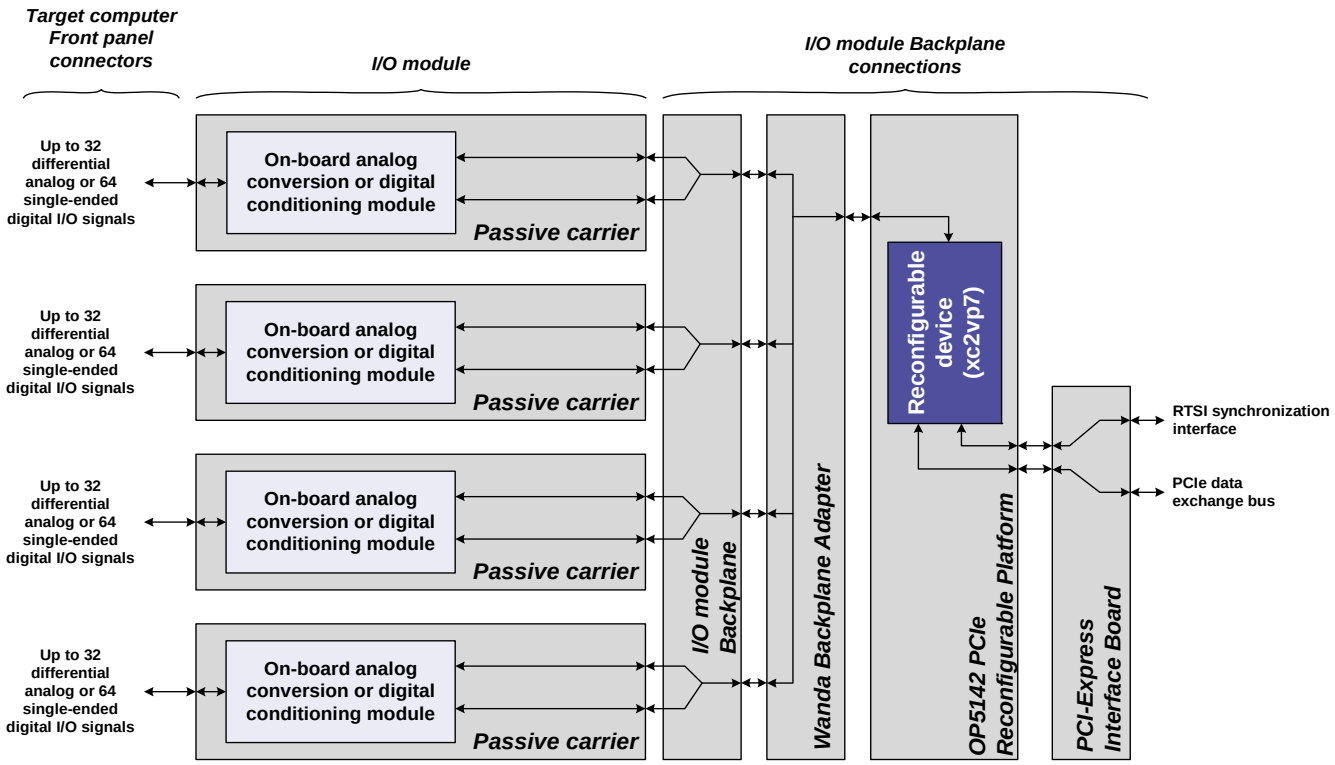
Target computer Front panel connectors
I/O module
I/O module Backplane connections
Up to 32 differential analog or 64 single-ended digital I/O signals
On-board analog conversion or digital conditioning module
Passive carrier
Up to 32 differential analog or 64 single-ended digital I/O signals
On-board analog conversion or digital conditioning module
Passive carrier
Up to 32 differential analog or 64 single-ended digital I/O signals
On-board analog conversion or digital conditioning module
Passive carrier
Up to 32 differential analog or 64 single-ended digital I/O signals
On-board analog conversion or digital conditioning module
Passive carrier
I/O module Backplane
Wanda Backplane Adapter
Reconfigurable device (xc2vp7)
OP5142 PCIe Reconfigurable Platform
PCI-Express Interface Board
RTSI synchronization interface
PCIe data exchange bus

Figure 2:Block diagram of the OP5142 PCIe Reconfigurable Platform connectivity features.

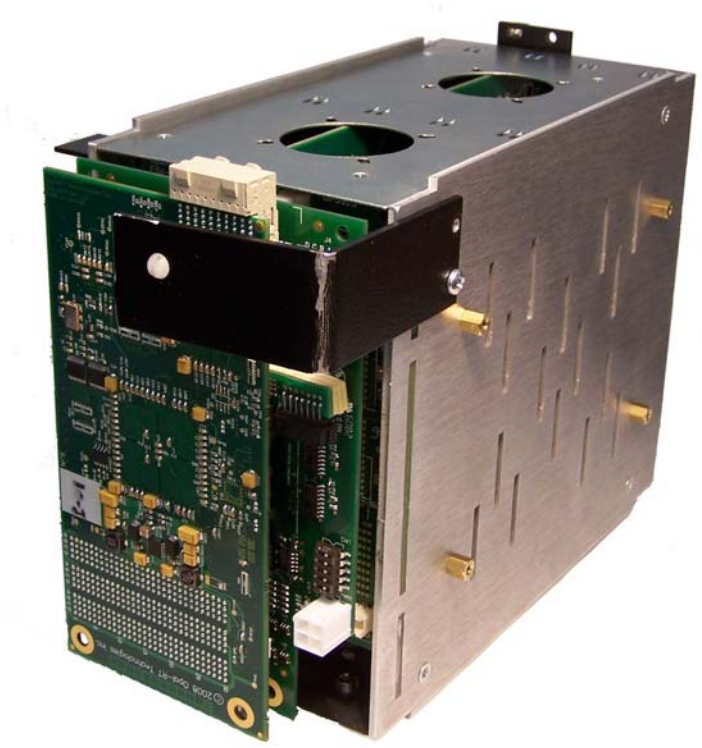

Figure 3:The OP5142 is stacked over the Wanda Backplane Adapter, which is an interface boars to the 4U I/O module itself.

4.2.1 Technical specifications

Digital I/O

Number of channels	256 input/output configurable in 1- to 32-bit groups
Compatibility	3.3V
Power-on state	High impedance/

FPGA

Device	Xilinx Spartan 3
I/O Package	fg676
Embedded RAM available	216 kbytes
Clock	100 MHz
Platform options	XC3S5000
Logic slices	33,280
Equivalent logic cells	74,880
Available I/O lines	489

Bus

Dimensions (not including connectors)	PCI-express x1
Data transfer	2.5 Gbit/s

4.2.2 Analog conversion interface

Two types of analog conversion modules are available: the OP5340 is a bank of analog-to-digital converters and the OP5330 is a bank of digital-to-analog converters. The analog conversion banks must be placed onto an OP5220 passive carrier, thus providing an easy access to the modules on the front panel of the Wanda box. OP5330 and OP5340 features are:

- Up to 16 analog Input (OP5340) or Output (OP5330) channels;
- One 16-bit ADC (OP5340) or DAC (OP5330) per channel;
- Simultaneous sampling on all channels eliminates skew errors inherent in multiplexed channels;
- Up to 500 kS/s update rate for every channel. Total throughput of up to 8 MS/s;
- Dynamic range of ± 16V;
- Accuracy of +/- 5mV;
- Hardware configurable on-board signal conditioning and anti-aliasing filter;
- On-board EEPROM memory for calibration parameters;
- Library of drag-and-drop Opal-RT RT-XSG blocks for Simulink (see Chapter 5).

Note: See Appendix B for more information on external port channel mapping.

4.2.3 Digital conditioning modules

Many types of digital conditioning modules are available to access the digital I/Os of the OP5142 user model:

- OP521X: a 64-channel digital conditioning module (32 inputs and 32 outputs). This conditioning module implements optocoupler-isolated lines that can accommodate I/O currents in the order of hundreds of milliamperes;
- OP5236-1: Differential LVDS digital conditioning module (16 inputs, 16 outputs);
- OP5236-2: Isolated TTL digital conditioning module (32 inputs, 32 outputs);
- OP5237-{1,2}: High Voltage Digital In/Out module (30 inputs, 32 outputs);
- Passthrough modules.

Building models with the RT-XSG toolbox

5

RT-XSG is a Matlab/Simulink toolbox developed by Opal-RT Technologies that enables an convenient way to create a programming file for the OP5142 programmable device. It is used in conjunction with the System Generator for DSP toolbox from Xilinx.

5.1 Access to the OP5142 board

The I/O components available from the Opal-RT OP5142 board can be accessed through a Simulink User model. Opal-RT Technologies provides an easy to use block set destined to communicate with the external conditioning and conversion modules (see Figure 4) and a CPU-based simulation subsystem. See the help file of each block for more information on how to interface them in the design, or refer to Appendix A.

Adding an interface to an analog or digital bank is as easy as dragging-and-dropping a block from the library into the design and feeding it with a signal with an appropriate numbering format. For the OP5142 platform, the user has access to up to 8 banks of up to 32 digital lines to communicate with analog and/or digital passive carriers attached to the backplane of the target computer. They are accessed via an “IO Block”, in which the designer indicates the location of the module that manages the signals.

In addition to the “IO Block”, the “DataIN” and “DataOUT” blocks enable the FPGA model to communicate data with an RT-Lab/Livelab-compatible CPU-based model.

The “Hardware Config” block is used to help the user determine where digital and/or analog signals can be accessed or routed.

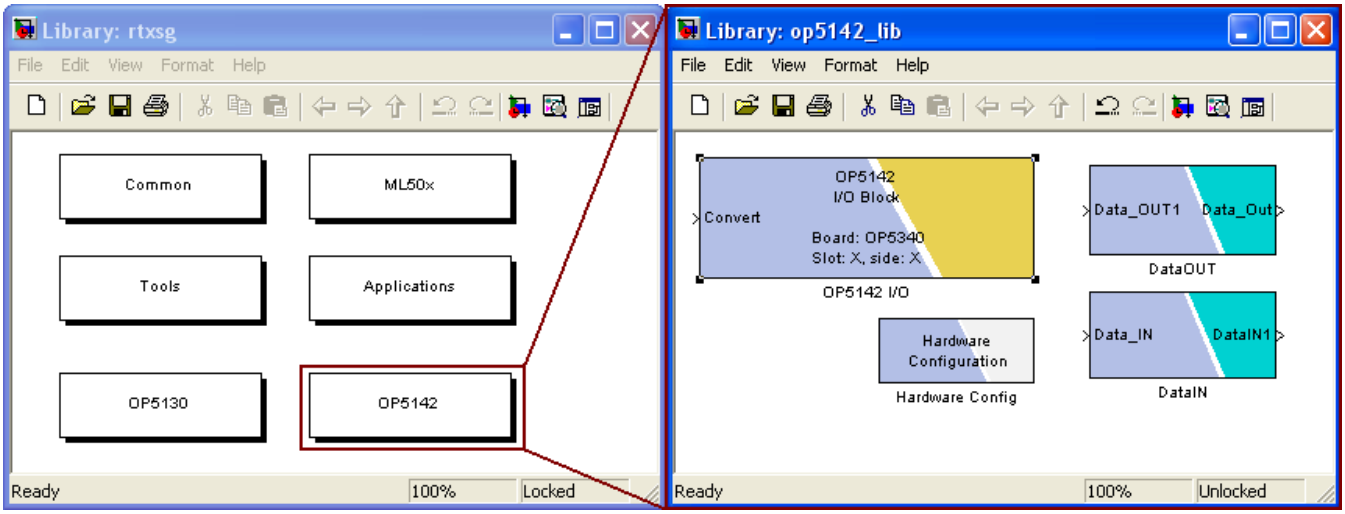

Figure 4:Opal-RT RT-XSG OP5142 block set.

5.2 Data type and rate management

Some Opal-RT RT-XSG library blocks have predefined input/output port fixed-point formats. These formats cannot be changed by the user as they must match the type expected from external modules ports, such as the ADC and DAC control signals. Refer to the blocks help file for further details.

In addition, the clock frequency of the OP5142 board is fixed to 100 MHz. Slower processing rates can be achieved by using downsampling and upsampling blocks from the System Generator for DSP Blockset. Note that he clock distribution is absent from the Simulink RT-XSG design as it is managed by the Xilinx and Opal-RT toolboxes. However, it is important to keep in mind the importance of the clock in hardware computing.

Note: Passing through a majority of blocks from the System Generator library induces a delay on the signals, ranging from picoseconds to tens of nanoseconds. It might be necessary to reduce the sampling rate of certain parts of the computation processes in order for that delay to become negligible.

5.3 Inserting custom VHDL modules in design

The easiest way to include a VHDL user model into the system is to instantiate it as a “black box” into the Simulink RT-XSG design. This method may facilitate the interface with Opal-RT conversion module controllers (ADC and DAC interfaces). Refer to the ‘Black box’ block help from the System Generator for DSP Blockset for more informations on how to configure a black box.

5.4 Generation of the programming file and target platform recompilation

The ‘Opal-RT FPGA Synthesis Manager’ block includes all the functionalities needed to compile the RT-XSG user model and to translate it into a programming file suitable for the reprogrammable device of the OP5142 board. The RT-LAB software environment enables the user to program the reconfigurable boards used by a simulation model using the configuration file generated via this block.

In order to generate the programming file, the following steps must be performed:

- Verify the correctness of the design using the “Update Diagram” button (Ctrl-D) from the Simulink toolbar and correct the errors, if any;
- Insert a ‘Opal-RT FPGA Synthesis Manager’ block into your design. In this block GUI (Figure 6), select the appropriate reprogrammable platform from the list and click the “Generate programming file” button. Programming file generation will take several minutes to complete.

Note: For a programming file to be generated, the user must set the “Rebuild option” parameter to ‘Always’ or ‘Only if changes needed’. This requirement is included to prevent unwanted compilations, as this operation can take from several minutes to several hours to complete, depending on the system characteristics.

After the generation of a valid programming file, the user can easily program the target platform by performing the following steps:

- Connect the target computer on the network using an ethernet cable so that it is accessible from the host computer;
- Power-up the target computer;
- Insert an “*Op Ctrl Reconfigurable IO*” block in an RT-LAB model that refers to the appropriate FPGA model (optional) and configuration file name (mandatory), as in Figure 5;

- Load an RT-LAB model from the RT-LAB controller environment, or from Livelab;
- Execute the model to enable FPGA-accelerated co-processing on the target computer.

Note: The programming file generation log information is written to the folder $Current_Directory/XSG Reports/<path to the current design>. Generation errors, including resource shortage or routing errors, can be found by parsing these files.

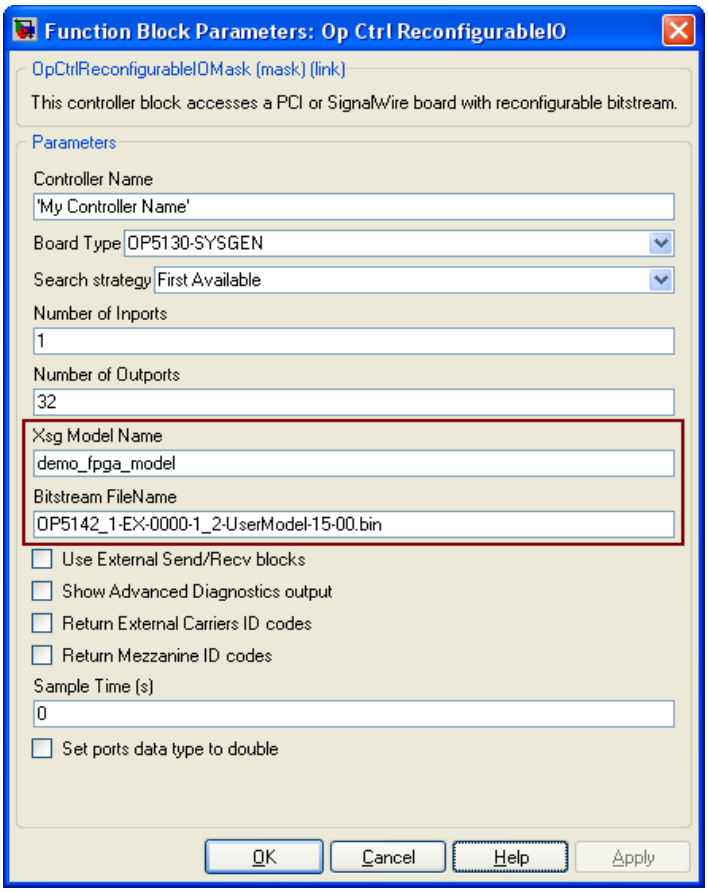

Figure 5:Example of *Op Ctrl Reconfigurable IO* block parameters. The “Xsg Model Name” parameter is optional, but the “Bitstream Filename” parameter is mandatory.

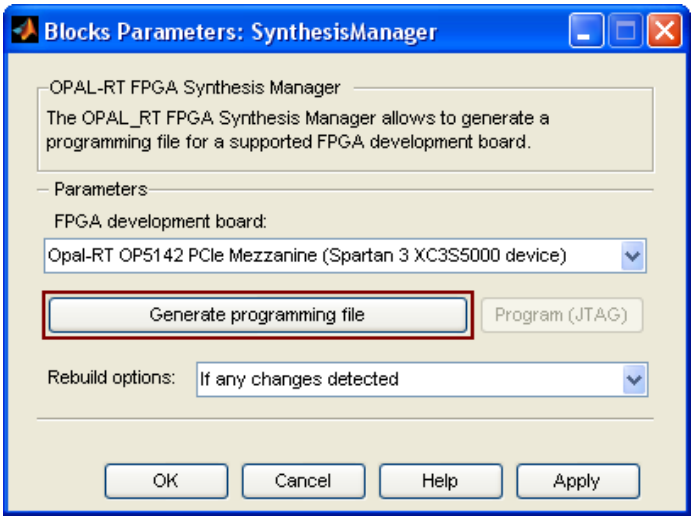

Figure 6:Opal-RT FPGA Synthesis Manager graphical user interface.

OPAL-RT

RT-XSG

Appendices

RTXSG-UG-11-03

IMAGINATION TO REAL-TIME

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OP5142 I/O Hardware Configuration Block

Library

RT-XSG/OP5142

Block

HardConfig

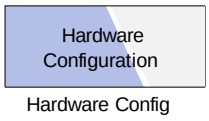


Figure 7:OP5142 Hardware Configuration Block.

Mask

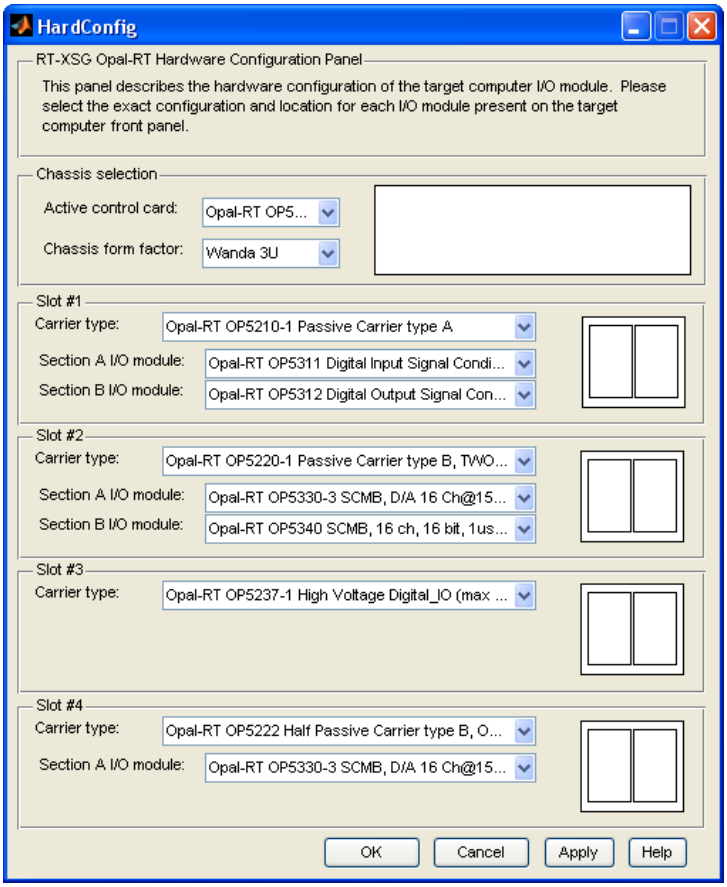

HardConfig
RT-XSG Opal-RT Hardware Configuration Panel
This panel describes the hardware configuration of the target computer I/O module. Please select the exact configuration and location for each I/O module present on the target computer front panel.
Chassis selection
Active control card:
Opal-RT OP5...
Chassis form factor:
Wanda 3U
Slot #1
Carrier type:
Opal-RT OP5210-1 Passive Carrier type A
Section A I/O module:
Opal-RT OP5311 Digital Input Signal Condi...
Section B I/O module:
Opal-RT OP5312 Digital Output Signal Con...
Slot #2
Carrier type:
Opal-RT OP5220-1 Passive Carrier type B, TWO...
Section A I/O module:
Opal-RT OP5330-3 SCMB, D/A 16 Ch@15...
Section B I/O module:
Opal-RT OP5340 SCMB, 16 ch, 16 bit, 1us...
Slot #3
Carrier type:
Opal-RT OP5237-1 High Voltage Digital_IO (max ...
Slot #4
Carrier type:
Opal-RT OP5222 Half Passive Carrier type B, O...
Section A I/O module:
Opal-RT OP5330-3 SCMB, D/A 16 Ch@15...
OK
Cancel
Apply
Help

Figure 8:OP5142 Hardware Configuration mask.

Description

The OP5142 Hardware Configuration Block is provided to help the user find the appropriate analog or digital, input or output signal interface on the Wanda 3 or Wanda 4 system. The user should specify in ths block the exact configuration of the Target PC I/O module.

Once this block is configured, the user may use a OP5142 I/O Block to access any I/O interface. The I/O Block provides the user with all the available signal interface board locations according to the requested signal type (analog or digital) and direction (input or output).

It is recommended that the user create a library with a preconfigured Hardware Configuration block for every RT-XSG compatible system available and include this library in the Matlab path and Simulink library Browser for easy configuration and updates of each design.

Parameters

Active Control Card: Select the type of active board on which the FPGA model is run (e.g. Opal-RT OP5142 Spartan 3 Mezzanine).

Chassis Form Factor: Select the chassis model name. This parameter is not used for hardware configuration but helps locate the available interfaces on the chassis picture.

Slot #1-4 Carrier Type: Select the type of 4U carrier located in the slot 1 to 4. It is recommended to indicate the carrier type of all non-empty slots. An empty slot is indicated by the <empty> choice and will not be available to OP5142 I/O blocks.

Slot #1-4 Section A I/O Module: For Type B carriers, a signal conditioning module can be placed on the carrier board. This parameter is provided to specify the appropriate mezzanine module for such boards (Section A).

Slot #1-4 Section B I/O Module: For Type B carriers, a signal conditioning module can be placed on the carrier board. This parameter is provided to specify the appropriate mezzanine module for such boards (Section B).

Inputs

This block has no input.

Outputs

This block has no output.

Characteristics and Limitations

This block has no special characteristics.

Direct Feedthrough	NO
Discrete sample time	NO
XHP support	N/A
Work offline	YES

OP5142 I/O Block

Library

RT-XSG/OP5142

Block

OP5142 I/O

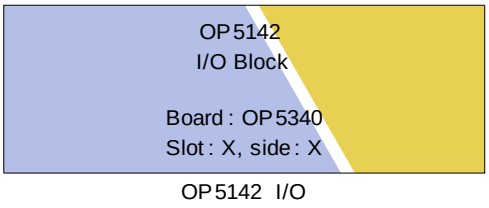


Figure 9:OP5142 I/O block.

Mask

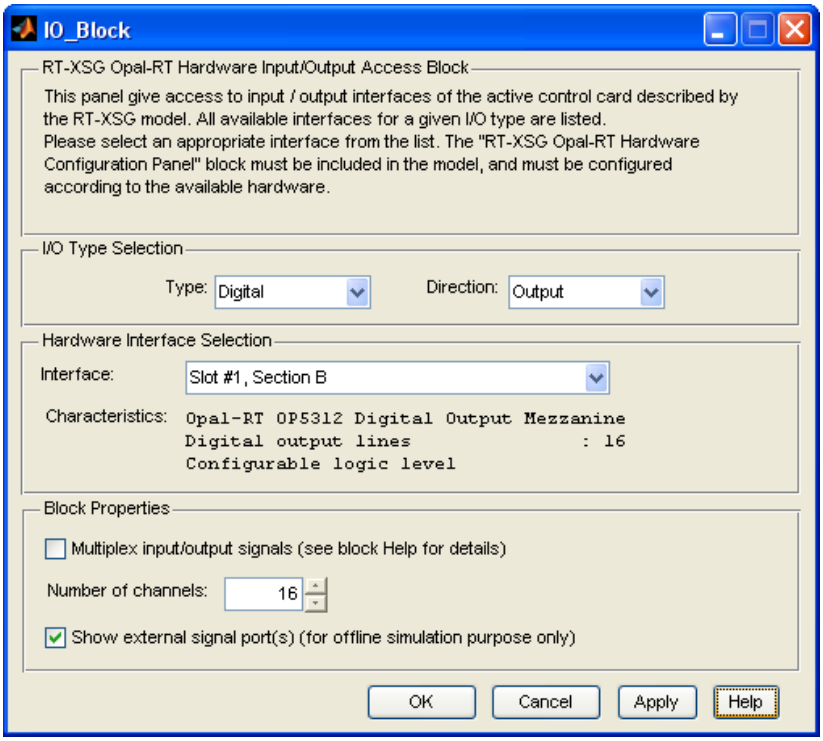

IO_Block
RT-XSG Opal-RT Hardware Input/Output Access Block
This panel give access to input / output interfaces of the active control card described by the RT-XSG model. All available interfaces for a given I/O type are listed.
Please select an appropriate interface from the list. The "RT-XSG Opal-RT Hardware Configuration Panel" block must be included in the model, and must be configured according to the available hardware.
I/O Type Selection
Type: Digital
Direction: Output
Hardware Interface Selection
Interface: Slot #1, Section B
Characteristics: Opal-RT OP5312 Digital Output Mezzanine
Digital output lines : 16
Configurable logic level
Block Properties
Multiplex input/output signals (see block Help for details)
Number of channels: 16
Show external signal port(s) (for offline simulation purpose only)
OK
Cancel
Apply
Help

Figure 10:OP6142 I/O block mask.

Description

This block gives access to all I/O modules controlled by the OP5142 active control card. It uses the OP5142 Hardware Configuration block to determine all the interface modules available according to the requested signal type (analog or digital) and direction (input or output). Implementation of the external connections is also available to enable offline

simulation of the complete system, including external hardware setup. Note that the block input and output ports strongly depend upon the selected interface board.

Parameters

Type: Type of signal to be interfaced (either analog or digital).

Direction: Direction of signal to be interfaced (either input or output).

Interface: This parameter drop-down menu lists all available interfaces available according to the selected “Type” and “Direction” parameters and the configuration of the ‘HardConfig’ block. The user chooses the appropriate interface to manage the specific signal.

Characteristics: This parameter is not editable. It shows the interface board characteristics for an easy identification of the board that corresponds to the selected interface location.

Multiplex input/output signals: This checkbox can be used to concatenate multiple input or output signals on the same Simulink net. This may help the user to build cleaner schematics. The behavior of this feature depends upon the type of signal interfaced:

- For digital signals, if this option is selected, the interface signal must be a multiple-bit fixed point format (e.g.: UFix16_0 may be used for a 16-bit multiplexed digital signal);
- For analog signals, if this option is selected, channels are multiplexed two by two, with a “valid” bit added. For example, the UFix33_0 format may be used for two analog output channels, the 16 LSBs being the first channel (in a format equivalent to the UFix16_11 numeric format), the next 16 bits being the second channel (also in a format equivalent to the UFix16_11 numeric format), and the MSB being the “Valid” bit. This format is useful for an easy connection to a DataIN or DataOUT block.

Note that for inputs, multiplexed signals are always in an unsigned fixed-point format with the binary point at position 0 (i.e. a positive integer format). Also, note that the external digital signals provided for offline simulation correspond to the multiple-bit fixed-point number interfaced by this block, and that the external analog signals for offline simulations are available in a channel-by-channel basis only.

Number of channels: This parameter is used to select the number of channels to appear on the block icon. This option is not available when the “Multiplex input/output signal” option is selected. In this case, the channel number is set to the maximal value allowed by the selected interface board

Show external signal port(s): This checkbox is used to add input or output ports to the block that represent the external world, from the active control card point of view. These ports can be used to connect the signals to a model of the external device connected to the signal conditioning modules. This feature can be very useful for offline simulation of the FPGA model.

Inputs

The block inputs strongly depend upon the parameters chosen in the block mask, and particularly upon the interface board used to conditionate the signals:

Analog input interface:

Convert: Convert input signal. Connect this input to the ModelSync “From” for synchronization with an external master device or provide a asynchronous sync source. If an asynchronous source is used, it must generate a 10-ns pulse. The maximum period between two pulses is 2µs (maximum conversion speed of a channel).

Ch{0-15}_external: These signals correspond to the external-world inputs of the analog-to-digital conversion module. They are used only for offline simulation, and appear only if the “Show external signal port(s)” option is selected in the block mask. They can be in a floating-point format.

Analog output interface:

Convert: Convert input signal. Connect this input to the ModelSync “From” for synchronization with an external master device or provide a asynchronous sync source. If an asynchronous source is used, it must generate a 10-ns pulse. The maximum period between two pulses is 1µs (maximum conversion speed of a channel). To have a synchronization of all the channels at the output of the adigital-to-analog conversion card, all data samples should be presented in sync with the Convert signal.

Ch{0-15}: These ports are the output signals to be sent to the digital-to-analog conversion module (if the “Multiplex input/output signals” option is not selected). These signals represent the voltage of the module outputs. Note that these inputs are converted automatically to a Fix16_11 numerical format. Signals outside the [-16, 15.9995] dynamic range will be wrapped in to a number in the range. Signals with a resolution higher than 0.0005V will lose precision.

Ch{1-15}_Ch{0-14}: These ports are the *multiplexed* output signals to be sent to the digital-to-analog conversion module (if the “Multiplex input/output signals” option is selected). These signals represent the voltage of the module outputs and must be in the UFix33_0 format. The 16 LSBs correspond to the first channel (in a format equivalent to the Fix16_11 numerical format), the next 16 bits to the second channel (also in a format equivalent to the Fix16_11 numerical format), and the MSB to a “Valid” bit (this bit is unused for analog output interfaces).

Digital input conditioning interface:

Ch{0-15}_external: These signals correspond to the external-world inputs of the digital conditioning module (if the “Multiplex input/output signals” option is not selected). They are used only for offline simulation, and appear only if the “Show external signal port(s)” option is selected in the block mask. They can be in a floating-point format.

DInput_external: This signal corresponds to the external-world inputs of the digital conditioning module (if the “Multiplex input/output signals” option is selected). It is used only for offline simulation, and appears only if the “Show external signal port(s)” option is selected in the block mask. It can be in a floating-point format.

Digital output conditioning interface:

Ch{0-15}: These ports are the output signals to be sent to the digital conditioning module (if the “Multiplex input/output signals” option is not selected). These signals must be 1-bit wide.

DOutput: This port corresponds to the output signals to be sent to the digital conditioning module (if the “Multiplex input/output signals” option is selected). It is a concatenation of the digital output channels. Missing bits are padded by zeros, if the signal connected to this port have fewer bits than the interface module capacity.

Digital passthrough interface:

Direction: This signal corresponds to the direction of the digital passthough lines. Its width must be equal to the passthrough interface module capacity (missing bits are padded with zeros). Zeros correspond to an outbound direction while ones correspond to an inbound direction.

DOutput: This port corresponds to the output signals to be sent to the digital conditioning module. It is a concatenation of the digital output channels. Missing bits are padded by zeros, if the signal connected to this port have fewer bits than the interface module capacity, and lines that correspond to inbound signals (as indicated by the signal connected to the “Direction” port) are unused.

DInput_external: This signal corresponds to the external-world inputs of the digital conditioning module (if the “Multiplex input/output signals” option is selected). It is used only for offline simulation, and appears only if the “Show external signal port(s)” option is selected in the block mask. It can be in a floating-point format.

Outputs

The block outputs strongly depend upon the parameters chosen in the block mask, and particularly upon the interface board used to conditionate the signals:

Analog input interface:

Ch{0-15}: These ports are the input signals received from the analog-to-digital conversion module (if the “Multiplex input/output signals” option is not selected). These signals represent the voltage of the module inputs. Note that these outputs are in the Fix16_11 numerical format, giving them a dynamic range of [-16, 15.9995] and a resolution of 0.0005V.

Ch{1-15}_Ch{0-14}: These ports are the *multiplexed* input signals received from the analog-to-digital conversion module (if the “Multiplex input/output signals” option is selected). These signals represent the voltage of the module inputs and are in the UFix33_0 format. The 16 LSBs correspond to the first channel (in a format equivalent to the Fix16_11 numeric format), the next 16 bits to the second channel (also in a format equivalent to the Fix16_11 numeric format), and the MSB to a “Valid” bit (active when the 32 LSBs are updated).

Analog output interface:

Ch{0-15}_external: These signals correspond to the external-world outputs of the digital-to-analog conversion module. They are used only for offline simulation, and appear only if the “Show external signal port(s)” option is selected in the block mask. They are in the “double” floating-point format.

Digital input conditioning interface:

Ch{0-15}: These ports are the input signals received from the digital conditioning module (if the “Multiplex input/output signals” option is not selected). They are 1-bit wide unsigned signals.

DInput: This port corresponds to the input signals received from the digital conditioning module (if the “Multiplex input/output signals” option is selected). It is is a concatenation of the digital input channels. The signal width is equal to the interface module capacity.

Digital output conditioning interface:

Ch{0-15}_external: These signals correspond to the external-world inputs of the digital conditioning module (if the “Multiplex input/output signals” option is not selected). They are used only for offline simulation, and appear only if the “Show external signal port(s)” option is selected in the block mask. They are in the “double” floating-point format.

DOutput_external: This signal corresponds to the external-world outputs of the digital conditioning module (if the “Multiplex input/output signals” option is selected). It is used only for offline simulation, and appears only if the “Show external signal port(s)” option is selected in the block mask. It is in the “double” floating-point format.

Digital passthrough interface:

DInput: This port corresponds to the input signals received from the digital conditioning module. It is a concatenation of the digital input channels. Its width corresponds to the interface module capacity, and lines that correspond to outbound bound signals (as indicated by the signal connected to the “Direction” port) are equal to the correspoding line of the signal connected to the “DInput” port.

DOutput_external: This signal corresponds to the external-world outputs of the digital conditioning module. It is used only for offline simulation, and appears only if the “Show external signal port(s)” option is selected in the block mask. It is in the “double” floating-point format.

Characteristics and Limitations

This block has no special characteristics.

Direct Feedthrough	NO
Discrete sample time	NO
XHP support	N/A
Work offline	YES

DataIN

Library

RT-XSG/OP5142

Block

DataIN

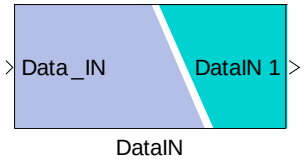


Figure 11:DataIN block.

Mask

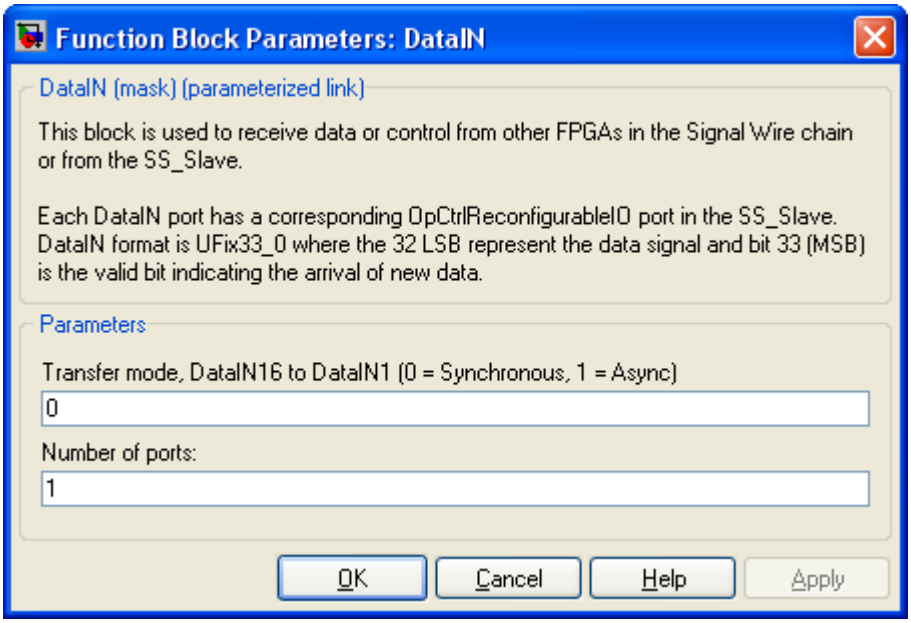

Function Block Parameters: DataIN
DataIN (mask) (parameterized link)
This block is used to receive data or control from other FPGAs in the Signal Wire chain or from the SS_Slave.
Each DataIN port has a corresponding OpCtrlReconfigurableIO port in the SS_Slave. DataIN format is UFix33_0 where the 32 LSB represent the data signal and bit 33 (MSB) is the valid bit indicating the arrival of new data.
Parameters
Transfer mode, DataIN16 to DataIN1 (0 = Synchronous, 1 = Async)
0
Number of ports:
1
OK
Cancel
Help
Apply

Figure 12:DataIN mask.

Description

This block represents the input link to the FPGA through the PCIe bus. Data may be coming from the target PC CPU model or from a previous FPGA in a multiple chip design. Up to thirty-two input ports are provided to the user for data samples and control signal transfers. One of the functions of this block is to perform data conversion from uint32 to the System Generator UFix33_0 data format. It is up to the user to extract the desired data out of the 32 least significant bits and to reinterpret these bits to the desired format (signed or unsigned with or without binary point).

This block is linked to the inputs of the RT-LAB OpCtrl Reconfigurable IO block found in the RT-LAB CPU model: port #1 of the OpCtrlReconfigurableIO corresponds to DataIN1, port #2 to DataIN2, etc.

Parameters

Transfer Mode: The buffering type allows a user to choose whether the incoming data is sent in the synchronous mode, where only one data sample can be transfered per calculation step, or in the asynchronous mode, where up to 254 samples can be transfered per calculation step. For example, a value of 010000000000101 in this field sets input ports 1 and 3 and 15 (MSB to LSB port representation) to the asynchronous mode.

Number of ports: This parameter allows the user to use multiple data ports to communicate information to parallel processors. When the number of ports is changed, the length of the “Transfer Mode” string is updated accordingly.

Inputs

Data_IN: This is a vector of uint32 type signals (with a length equal to the number of ports). Each of these signals represents an input port on the OpCtrlReconfigurableIO block of the RT-LAB CPU model. It is used for offline simulation only.

Outputs

DataIN{1,...,32}: Each of these ports is in the UFix33_0 format where the first 32 bits represent the data and bit 33 (the most significant bit) is the valid signal indicating when the information is updated. When in synchronous mode (default) the valid bit is in sync with the ModelSync train pulses (active high for 10 ns). In asynchronous or in burst mode, this bit is active on each arrival of the data.

Characteristics and Limitations

This block has no special characteristics.

Direct Feedthrough	NO
Discrete sample time	NO
XHP support	N/A
Work offline	YES

DataOUT

Library

RT-XSG/OP5142

Block

DataOUT

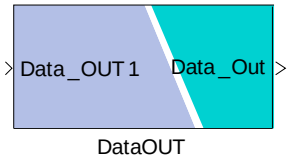


Figure 13:DataOUT block

Mask

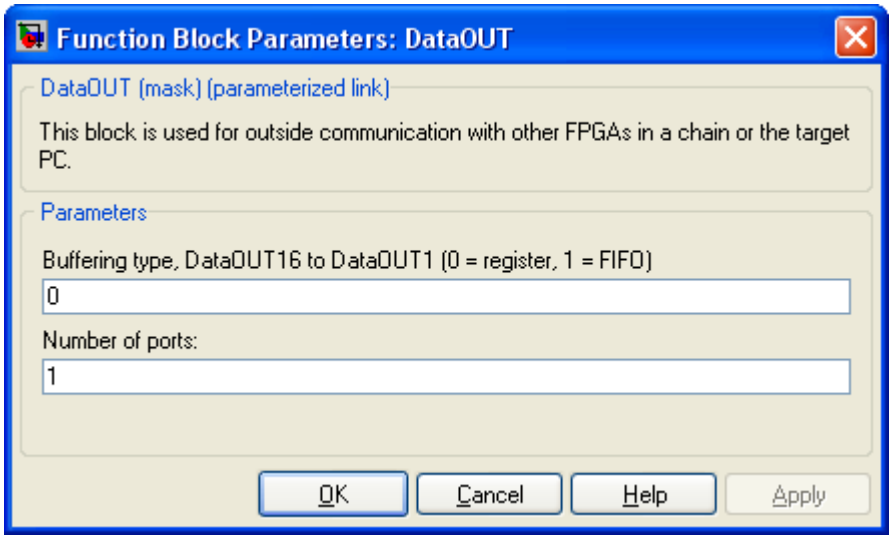


Figure 14:DataOUT mask.

Description

This block represents the output data link from the FPGA through the PCIe bus. Data may be going to the target PC (RT-LAB CPU model) or to another FPGA board in a multiple chip design (only RT-LAB CPU models are supported in this version). A maximum of thirty-two output ports are provided to the user for data samples and control signal transfers. One of the functions of this block is to do data conversion from the Xilinx System Generator UFix or Fix format to the uint32 data format.

This block is linked to the output ports of the OpCtrl ReconfigurableIO block found in the RT-LAB CPU model: port #1 of the OpCtrlReconfigurableIO block corresponds to DataOUT1, port #2 to DataOUT2, etc.

Parameters

Transfer Mode: The buffering type allows a user to choose whether to buffer the information in a single register where only one data sample can be transfered per calculation step or in a FIFO buffer-based mode where up to 254 samples can be transfered per calculation step. For example, a value of 010000000000101 in this field sets a FIFO on DataOUT ports 1 and 3 and 15 (MSB to LSB port representation). In FIFO mode, the number of samples stored is determined by the number of 10 ns pulses (one FPGA clock cycle) on bit 32 (MSB) of the port in FIFO mode per calculation step.

Number of ports: This parameter allows the user to use multiple data ports to communicate information with parallel processors. When the number of ports is changed, the length of the “Transfer Mode” string is updated accordingly.

Inputs

Data_OUT{1,...,32}: Each of these ports is in the UFix33_0 format where the first 32 bits represent the data and bit 33 (the most significant bit) is the valid signal indicating when the data is ready. Bit 33 can be seen as a write signal to the buffer, whether it be a register or a FIFO, in the DataOUT block. Each of those buffers is emptied and transfered to the CPU model at the beginning of each calculation step.

Outputs

DataOUT: This is a vector of signals in the uint32 format (with a length equal to the number of ports). Each one of these signals represents an output port on the OpCtrlReconfigurableIO block in the RT-LAB CPU model. This port is used for offline simulation only.

Characteristics and Limitations

This block has no special characteristics.

Direct Feedthrough	NO
Discrete sample time	NO
XHP support	N/A
Work offline	YES (No for ports set in FIFO mode)

OP5142 Active Controller signal description

B

This appendix documents the interface signals to the OP5142 connectors. Refer to Figure 15 to locate these connectors.

Important: The user should not need to access directly the signals from the OP5142 board, and should not modify the hardware configuration set during manufacturing by adding jumpers or modifying their position, nor by changing the board ID.

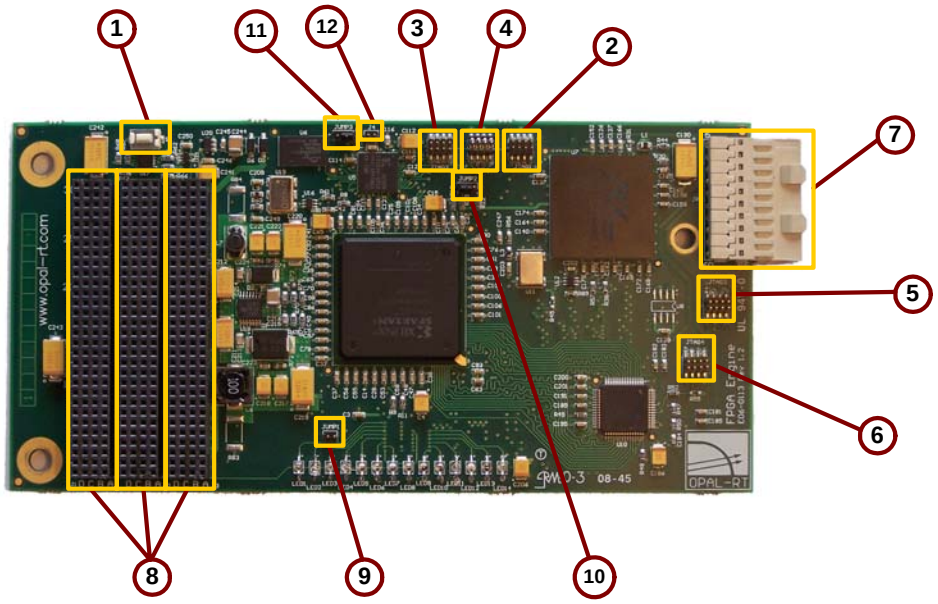


Figure 15:OP5142 layout and connectors.

Legend:

#	Name	Description	#	Name	Description
1	S1	FPGA Engine manual reset	**7**	JP1	PCIe & Synchronization bus and Power supply
2	JTAG1	FPGA JTAG interface	**8**	J1/J2/J3	Backplane data, ID and I²C interface
3	JTAG2	CPLD JTAG interface	**9**	JUMP1	Identification EEPROM write protection
4	JUMP4	JTAG Architecture selection	**10**	JUMP2	FPGA Configuration mode selection
5	JTAG3	PCIe Bridge JTAG interface	**11**	JUMP3	Flash memory Write protection
6	JTAG4	SerDes JTAG interface	**12**	J4	Flash memory forced programmation voltage

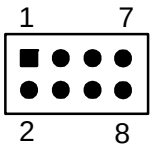
1. FPGA Engine manual reset

This button is connected to the master reset signal of the OP5142 board. Pressing this button forces the FPGA reconfiguration, and then sends a reset signal to all OP5142 subsystems.

2. FPGA JTAG interface

This connector give access to the OP5142 JTAG chain. It is used to configure the flash memory with its default configuration file. The JTAG connection enables the user to program manually the reprogram-mable components on the board and to debug the design using the Chipscope, through the System Generator for DSP “Chipscope” block. The use of this port is reserved for advanced users. In general,

this port should not be used after the board is manufactured. Depending upon the “JUMP4” jumper presence, this interface may give access to both the FPGA and CPLD configuration, or only the FPGA one. For all JTAG interfaces on the OP5142, the pinout is as follows:.



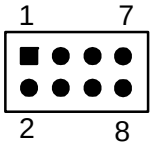
#	Pin Name	Description
1	TCK	Test Clock
2	TMS	Test Mode Select
3	TDI	Test Data Input (CPLD)
4		*Not connected*
5	TDO	Test Data Output (CPLD)
6		*Not connected*
7	GND	Ground
8	+3V3	Supply voltage

3. CPLD JTAG interface

If the “JUMP4” jumpers are set to the independent mode, this connector gives access to the CPLD JTAG configuration interface. The JTAG connection enables the user to program manually the reprogrammable components on the board. The use of this port is reserved for advanced users. In general, this port should not be used after the board is manufactured. If the jumpers are set to the shared mode, the CPLD and FPGA JTAG configuration are dasy-chained, and the “JTAG1” connector must be used instead of this one.

4. JTAG architecture selection

This connector enables the JTAG interface of the OP5142 CPLD and FGPA to be daisy-chained. For independent operation, place jumper between pins 6-8. For daisy chain operation, place jumpers between pins 1-2, 3-4, 5-6 ans 7-8, and use the FPGA JTAG connector only.



Position	Configuration Type
6-8 only	CPLD and FPGA are configured using independent JTAG circuitry (through JTAG1 and JTAG2, respectively).
1-2, 3-4, 5-6 & 7-8	CPLD and FPGA are configured using a shared JTAG circuitry (through JTAG1).
No jumper	JTAG configuration is not used.

5. PCIe Bridge JTAG interface

This connector give access to the PLX PCI-express bridge JTAG interface. It is used during manufacturing to configure the bridge with its default configuration, and should not be used by the user.

6. SerDes JTAG interface

This connector give access to the Texas Instrument Serializer-Deserializer JTAG interface. It is used during manufacturing to configure the chip with its default configuration, and should not be used by the user.

7. PCIe & Synchronization bus and Power Supply

This port implements all data and power transfers that need to be done with the external world. It carries to the external PCI-express adapter:

- The synchronization pulse train to a RTSI connector;
- Data communication packets to the PCI-express bus;
- Power supply voltages.

8. Backplane Data, ID and I²C interface

These three connectors are to be attached to the Wanda Backplane Adapter J1, J2 and J3 headers. They exchange all I/O-related data to the I/O module, including identification data, serial communication with I²C devices and user I/O dataflow.

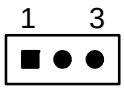
9. Identification EEPROM write protection

This header enables the write protection of the EEPROM located on the OP5142. This EEPROM contains the board revision ID, and should always remain write-protected.

Position	Configuration Type
Jumper	EEPROM is NOT write-protected.
No jumper	EEPROM is write-protected.

10. FPGA Configuration Mode selection

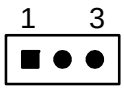
This header enables the developer to select the way the OP5142 FPGA should be configured. The two options are (a) JTAG configuration, or (b) Slave parallel configuration (from the Flash memory). In normal use, the FPGA should always be configured using the Slave parallel feature. Note that pin #1 is on the left-hand side of the header (i.e. the “J”UMP side).



Position	Configuration Type
1-2	Slave parallel mode reconfiguration.
2-3	JTAG mode reconfiguration.
No jumper	FPGA is never reconfigured.

11. Flash Memory write protection

This header is used to enable the developer to write some reserved sectors of the configuration flash memory. These sectors should never be used by the user.



Position	Configuration Type
1-2	All flash sectors are unprotected
2-3	Normal operation. Certain flash sectors are protected.
No jumper	FPGA configuration flash is never written.

12. Flash memory forced programmation voltage

This header provides a 12V supply voltage to the JUMP3 connector. JUMP3 is used to enable the developer to write some reserved sectors of the configuration flash memory. These sectors should never be used by the user. Note that pin #1 is on the left-hand side of the header (i.e. the “J”4 side).

#	Pin Name	Description
1	VCC	+12V
2	GND	*Ground*

Wanda Backplane Adapter signal description

This appendix documents the interface signals of the Wanda Backplane Adapter. Refer to Figure 16 to locate these connectors.

Important: The user should not need to access directly the signals from the Wanda Backplane adapter board except for the P1 connector, if available, and should not modify the hardware configuration set during manufacturing by changing the board ID.

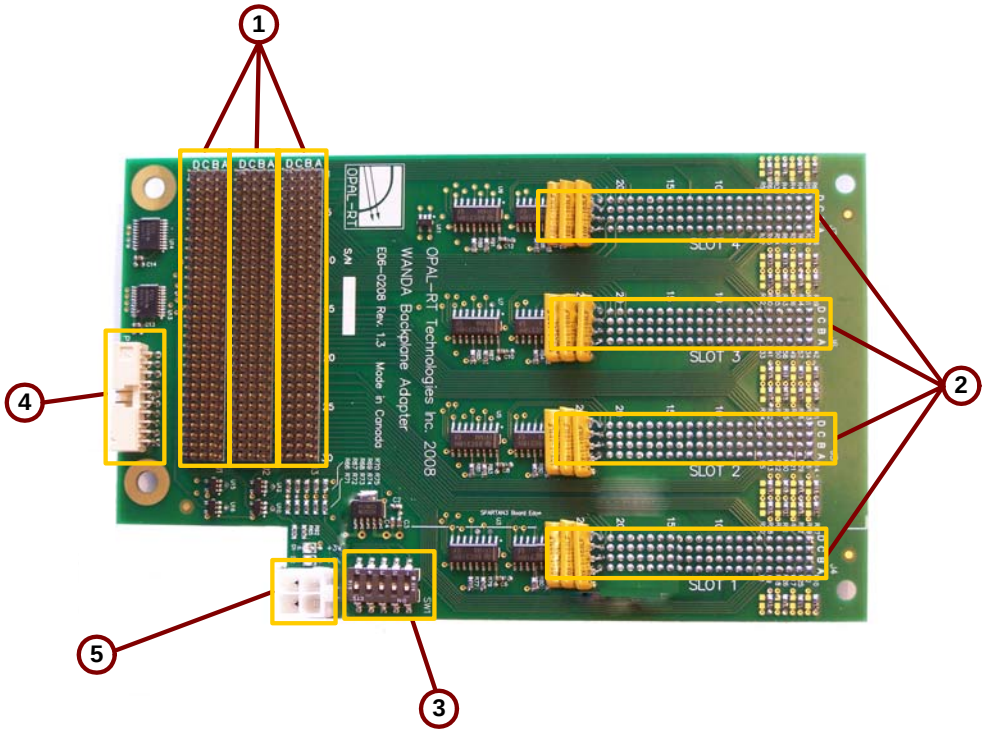


Figure 16:Wanda Backplane Adapter layout and connectors.

Legend:

#	Name	Description	#	Name	Description
1	J1/J2/J3	Active controller data, ID and I²C interface	**4**	P1	FPGA Unused pins.
2	J4/J5/J6/J7	Backplane data, ID and I²C interface	**5**	PWR1	Power supply
3	SW1	Module identification number			

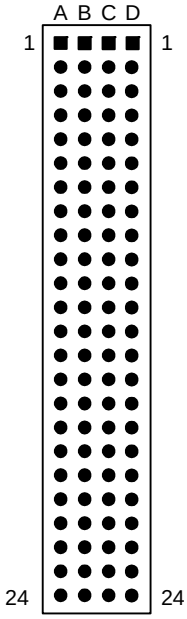
1. Active controller data, ID and I²C interface

These three headers are to be attached to the OP5142 Active controller J1, J2 and J3 connectors. They exchange all I/O-related data to the controller module, including identification data, serial communication with I²C devices and user I/O dataflow.

2. Backplane controller data, ID and I²C interface

These four connectors, which are located on the rear side of the Wanda Backplane Adapter, reroute the signals from the J1, J2 and J3 headers to connect them to the appropriate line of each I/O module through the Wanda Backplane. These signals should not be accessed directly by the user, The following

pinout may be used to develop new I/O modules. The pin layout is as viewed from the rear side of the adapter card.

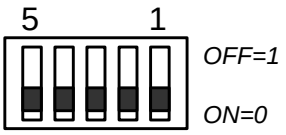


#	Pin Name	Description	#	Pin Name	Description
D1	EXT_A_SCL	Section A: I²C - Serial clock signal	**C1**	GND	*Ground*
D2	EXT_A_SDA	Section A: I²C - Serial data signal	**C2**	GND	*Ground*
D3	EXT_A_A2	Section A: I²C - Adress bit 2	**C3**	EXT_A_A1	Section A: I²C - Adress bit 1
D4	EXT_A_A0	Section A: I²C - Adress bit 0	**C4**	EXT_A_WP	Section A: I²C - Write protect
D5	GND	*Ground*	**C5**	EXT_A_IO_0	Section A: Data bit 0
D6	EXT_A_IO_1	Section A: Data bit 1	**C6**	EXT_A_IO_2	Section A: Data bit 2
D7	EXT_A_IO_3	Section A: Data bit 3	**C7**	EXT_A_IO_4	Section A: Data bit 4
D8	EXT_A_IO_5	Section A: Data bit 5	**C8**	EXT_A_IO_6	Section A: Data bit 6
D9	EXT_A_IO_7	Section A: Data bit 7	**C9**	EXT_A_IO_8	Section A: Data bit 8
D10	EXT_A_IO_9	Section A: Data bit 9	**C10**	EXT_A_IO_10	Section A: Data bit 10
D11	EXT_A_IO_11	Section A: Data bit 11	**C11**	EXT_A_IO_12	Section A: Data bit 12
D12	EXT_A_IO_13	Section A: Data bit 13	**C12**	EXT_A_IO_14	Section A: Data bit 14
D13	EXT_A_IO_15	Section A: Data bit 15	**C13**	EXT_A_IO_16	Section A: Data bit 16
D14	EXT_A_IO_17	Section A: Data bit 17	**C14**	EXT_A_IO_18	Section A: Data bit 18
D15	EXT_A_IO_19	Section A: Data bit 19	**C15**	EXT_A_IO_20	Section A: Data bit 20
D16	EXT_A_IO_21	Section A: Data bit 21	**C16**	EXT_A_IO_22	Section A: Data bit 22
D17	EXT_A_IO_23	Section A: Data bit 23	**C17**	EXT_A_IO_24	Section A: Data bit 24
D18	EXT_A_IO_25	Section A: Data bit 25	**C18**	EXT_A_IO_26	Section A: Data bit 26
D19	EXT_A_IO_27	Section A: Data bit 27	**C19**	EXT_A_IO_28	Section A: Data bit 28
D20	EXT_A_IO_29	Section A: Data bit 29	**C20**	EXT_A_IO_30	Section A: Data bit 30
D21	EXT_A_IO_31	Section A: Data bit 31	**C21**	GND	*Ground*
D22	EXT_A_ID5	Section A: Identification bit 5	**C22**	EXT_A_ID4	Section A: Identification bit 4
D23	EXT_A_ID3	Section A: Identification bit 3	**C23**	EXT_A_ID2	Section A: Identification bit 2
D24	EXT_A_ID1	Section A: Identification bit 1	**C24**	EXT_A_ID0	Section A: Identification bit 0

#	Pin Name	Description	#	Pin Name	Description
B1	EXT_B_SCL	Section B: I²C - Serial clock signal	**A1**	GND	*Ground*
B2	EXT_B_SDA	Section B: I²C - Serial data signal	**A2**	GND	*Ground*
B3	EXT_B_A2	Section B: I²C - Adress bit 2	**A3**	EXT_B_A1	Section B: I²C - Adress bit 1
B4	EXT_B_A0	Section B: I²C - Adress bit 0	**A4**	EXT_B_WP	Section B: I²C - Write protect
B5	GND	*Ground*	**A5**	EXT_B_IO_0	Section B: Data bit 0
B6	EXT_B_IO_1	Section B: Data bit 1	**A6**	EXT_B_IO_2	Section B: Data bit 2
B7	EXT_B_IO_3	Section B: Data bit 3	**A7**	EXT_BA_IO_4	Section B: Data bit 4
B8	EXT_B_IO_5	Section B: Data bit 5	**A8**	EXT_B_IO_6	Section B: Data bit 6
B9	EXT_B_IO_7	Section B: Data bit 7	**A9**	EXT_B_IO_8	Section B: Data bit 8
B10	EXT_B_IO_9	Section B: Data bit 9	**A10**	EXT_B_IO_10	Section B: Data bit 10
B11	EXT_B_IO_11	Section B: Data bit 11	**A11**	EXT_B_IO_12	Section B: Data bit 12
B12	EXT_B_IO_13	Section B: Data bit 13	**A12**	EXT_B_IO_14	Section B: Data bit 14
B13	EXT_B_IO_15	Section B: Data bit 15	**A13**	EXT_B_IO_16	Section B: Data bit 16
B14	EXT_B_IO_17	Section B: Data bit 17	**A14**	EXT_B_IO_18	Section B: Data bit 18
B15	EXT_B_IO_19	Section B: Data bit 19	**A15**	EXT_B_IO_20	Section B: Data bit 20
B16	EXT_B_IO_21	Section B: Data bit 21	**A16**	EXT_B_IO_22	Section B: Data bit 22
B17	EXT_B_IO_23	Section B: Data bit 23	**A17**	EXT_B_IO_24	Section B: Data bit 24
B18	EXT_B_IO_25	Section B: Data bit 25	**A18**	EXT_B_IO_26	Section B: Data bit 26
B19	EXT_B_IO_27	Section B: Data bit 27	**A19**	EXT_B_IO_28	Section B: Data bit 28
B20	EXT_B_IO_29	Section B: Data bit 29	**A20**	EXT_B_IO_30	Section B: Data bit 30
B21	EXT_B_IO_31	Section B: Data bit 31	**A21**	GND	*Ground*
B22	EXT_B_ID5	Section B: Identification bit 5	**A22**	EXT_B_ID4	Section B: Identification bit 4
B23	EXT_B_ID3	Section B: Identification bit 3	**A23**	EXT_B_ID2	Section B: Identification bit 2
B24	EXT_B_ID1	Section B: Identification bit 1	**A24**	EXT_B_ID0	Section B: Identification bit 0

3. Module identification number

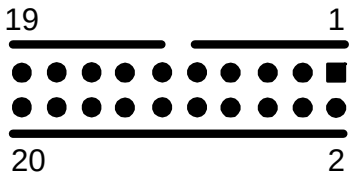
These switches set the Wanda Backplane Adapter module identification number. It should be configured correctly on arrival from manufacture, and should not be modified afterwards.



#	Pin Name	Description
1	MOD_ID_0	Module identification number, bit 0
2	MOD_ID_1	Module identification number, bit 1
3	MOD_ID_2	Module identification number, bit 2
4	MOD_ID_3	Module identification number, bit 3
5	MOD_ID_4	Module identification number, bit 4

4. FPGA unused pins

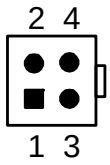
This connector gives access to unused pins of the Active Controller FPGA. If it is available, the FPGA signal pin assignation is as follows:



#	Pin Name	Description	#	Pin Name	Description
1	SYS_RST	CPLD-generated System reset signal	**2**	CLK1	Unused signals - bit 0
3	BPP1_1	Unused signals - bit 1	**4**	BPP1_2	Unused signals - bit 2
5	BPP1_3	Unused signals - bit 3	**6**	BPP1_4	Unused signals - bit 4
7	BPP1_5	Unused signals - bit 5	**8**	BPP1_6	Unused signals - bit 6
9	BPP1_7	Unused signals - bit 7	**10**	BPP1_8	Unused signals - bit 8
11	BPP1_9	Unused signals - bit 9	**12**	BPP1_10	Unused signals - bit 10
13	BPP1_11	Unused signals - bit 11	**14**	BPP1_12	Unused signals - bit 12
15	BPP1_13	Unused signals - bit 13	**16**	BPP1_14	Unused signals - bit 14
17	BPP1_15	Unused signals - bit 15	**18**	BPP1_16	Unused signals - bit 16
19	GND	*Ground*	**20**	GND	*Ground*

5. Power supply

This connector powers the Wanda backplane adapter



#	Pin Name	Description
1	GND	*Ground*
2	GND	*Ground*
3	VCC	*+5V power supply*
4	VCC	*+5V power supply*